High-performance Multiplexing with the DG408

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The DG408 and DG409, new multiplexers from Siliconix, represent a new generation of high-performance multiplexers and demultiplexers with many specific improvements over existing products available today. Built with the company's high-voltage silicon-gate technology, these new ICs offer *significantly* reduced on-resistance ($<100 \, \Omega$), leakage currents ($I_{S(OFF)} < 0.5 \, nA$), power dissipation (2.25 mW), and much faster switching (250 ns) over older industry standards. These improved specifications allow designers to greatly reduce system errors and improve system performance.

The DG408 and DG409 will enhance two primary multiplexer and demultiplexer applications: communications and telemetry. Important multiplexer specifications depend on the application and the accuracy required by the system. For example, in communications, switching speed is important; whereas, in telemetry, on-resistance, charge injection, and output capacitance are critical because they determine the accuracy of the system. This article will present examples of these types of applications and discuss the benefits that these new multiplexers bring to their system performance.

Communications

The digital telephone exchange is a communication multiplexed system. In this type of system (see Figure 1), a number of telephone channels carrying speech are sequentially switched (i.e., multiplexed) for fixed periods of time into an analog-to-digital converter. Once converted to a digital form, the different speech signals can be processed and routed within the exchange.

A typical specification for the voice bandwidth in a telephone exchange is 3.3 kHz. For this bandwidth, an 8-kHz sampling rate is sufficient (i.e., sampling rate > 2 times the bandwidth). Therefore, each sampling period is 125 μs, during which time, each of the 32 channels of the multiplexer must be addressed. This means that each channel will be turned on for 3.906 μs (125 μs/32). This figure is ideal, since the multiplexer cannot switch in zero time. Depending on the particular multiplexer used, there will either be an overlap between sampling pulses (i.e., make-before-break switching), which leads to crosstalk between channels, or a separation between samples (i.e.,

break-before-make switching), which reduces the sampling time of a particular channel and results in lower multiplexer efficiency. The DG408 has switching times (250 ns) guaranteed to be more than four times faster than previously available (1 μs) multiplexers. Its guaranteed break-before-make time (10 ns) prevents crosstalk during switching transitions.
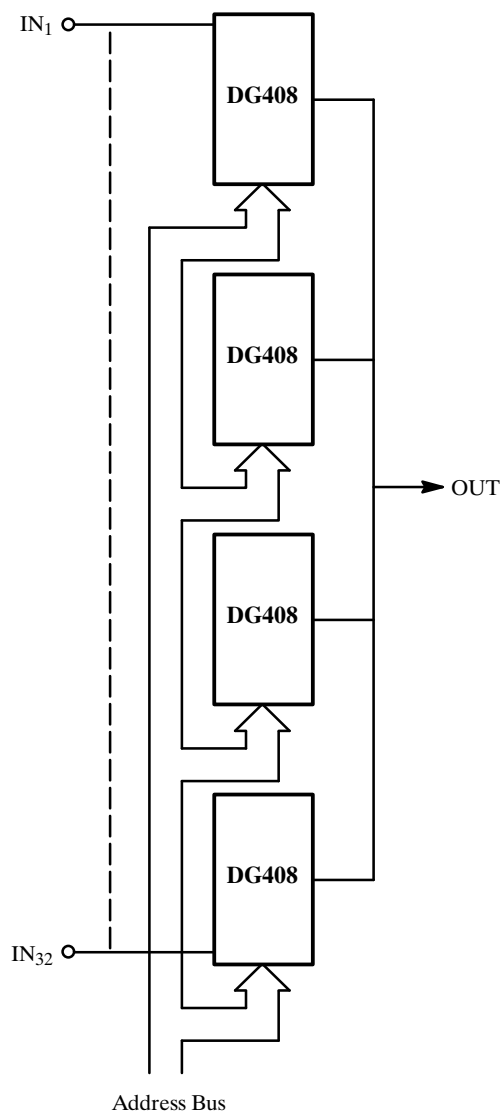

Figure 1. 32-Channel Multiplexed System

Telemetry

Telemetry offers many applications for multiplexer and demultiplexer combinations. A telemetry system uses transducers (a device which converts a physical variable, such as pressure, flow, temperature, etc. to an electrical equivalent) to measure variables, which are fed back via a multiplexer, monitored, and acted upon if necessary.

Figure 2 shows the position of a multiplexer in a high-performance, closed-loop telemetry system. The transducer output generally produces an analog output (which may need preamplification and filtering prior to multiplexing). With a wide variety of transducer types available, the inputs to the multiplexer may take many forms, including high-frequency, dc, high-level, low-level, voltage, current, and differential signals. Whether a signal requires preconditioning before being multiplexed depends on the total accuracy required of the system.

Because the multiplexer follows the transducer output, the multiplexer specification will have a significant bearing on the system accuracy. For example, a low-level signal can, potentially, require preamplification. A primary source of error with a low-level signal may be the switching transients present in the multiplexer. These transients are the result of charge injection from the switches, producing an error voltage (usually positive for a CMOS switch) which appears at the multiplexer output. Hence, the lower the signal level, the greater the error introduced by the charge injection of the switch.

For example, the DG408 with its 20-pC (typical) charge injection will create a 20-mV offset error when switching into a 1000-pF load. For low-level signals, this offset may be excessive. Using a differential multiplexer, such as the DG409, will provide at least an order of magnitude improvement in the total offset error.

High-level signals become a potential problem at different values, depending on the technology used to manufacture the multiplexer. For a CMOS multiplexer, high-level signals greater than the positive and negative supplies must be avoided to prevent permanent damage to the device. If the supplies are exceeded by the analog signal, the inherent source/drain-to-supply diodes (Figure 3) will become forward biased.

When the expected overloads have a short duration, usually a couple of switching diodes used in series with the supply leads will prevent permanent damage by blocking the flow of reverse current in the power supply loads.

Differential signals can be generated by bridge-type transducers. These devices will produce a signal of two components: a common-mode signal which is large and a small difference signal. It is the difference component that conveys the measurement information. Figure 4 shows the DG409 differential multiplexer being buffered by a full differential amplifier which rejects the unwanted common-mode voltage. The amplifier output consists solely of the differential signal. The ability of the differential multiplexer to reject unwanted common-mode voltages makes it especially useful in systems where pick-up of electrical noise is a concern.
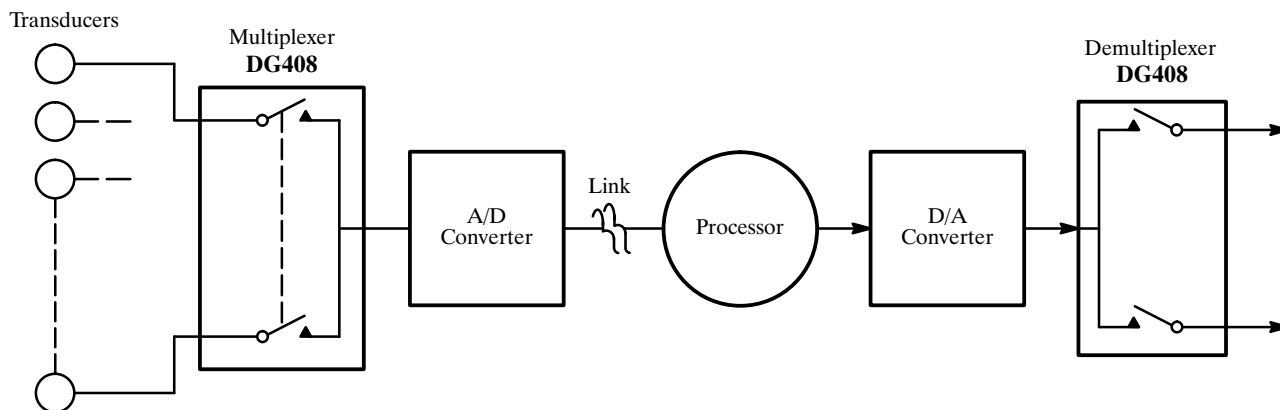

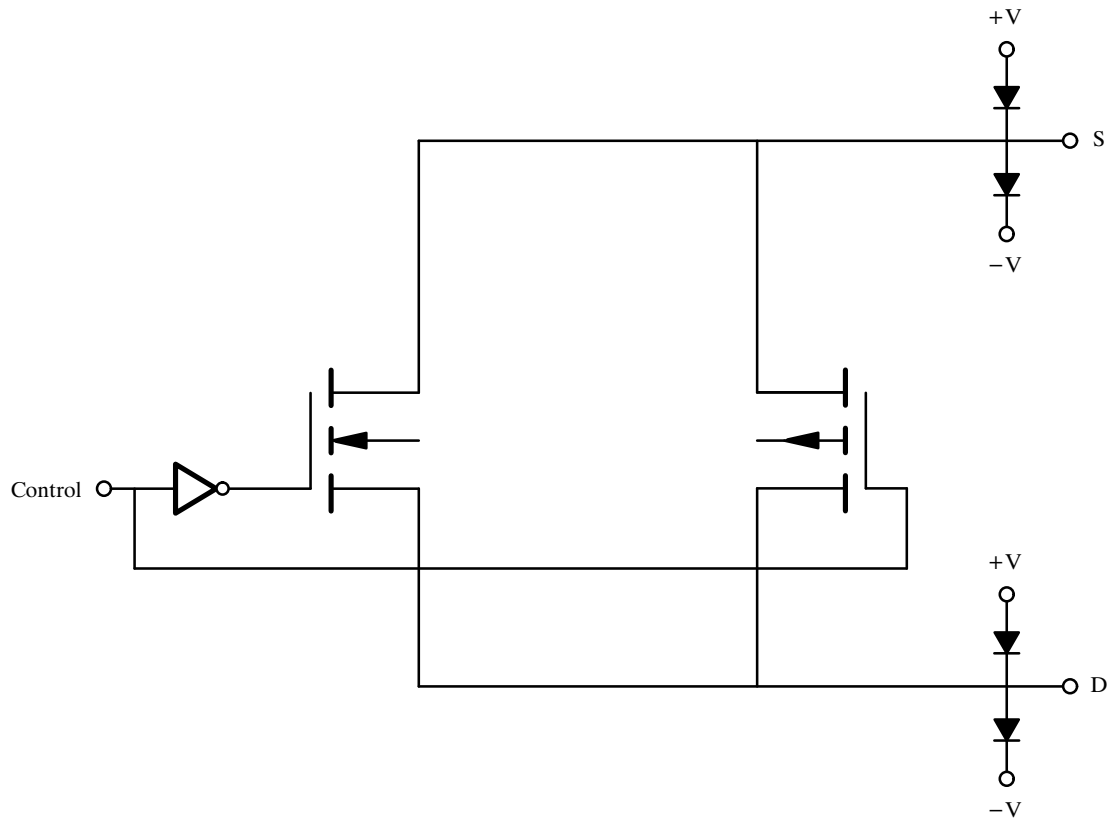**Figure 2.** Position of the Multiplexer in a Telemetry System
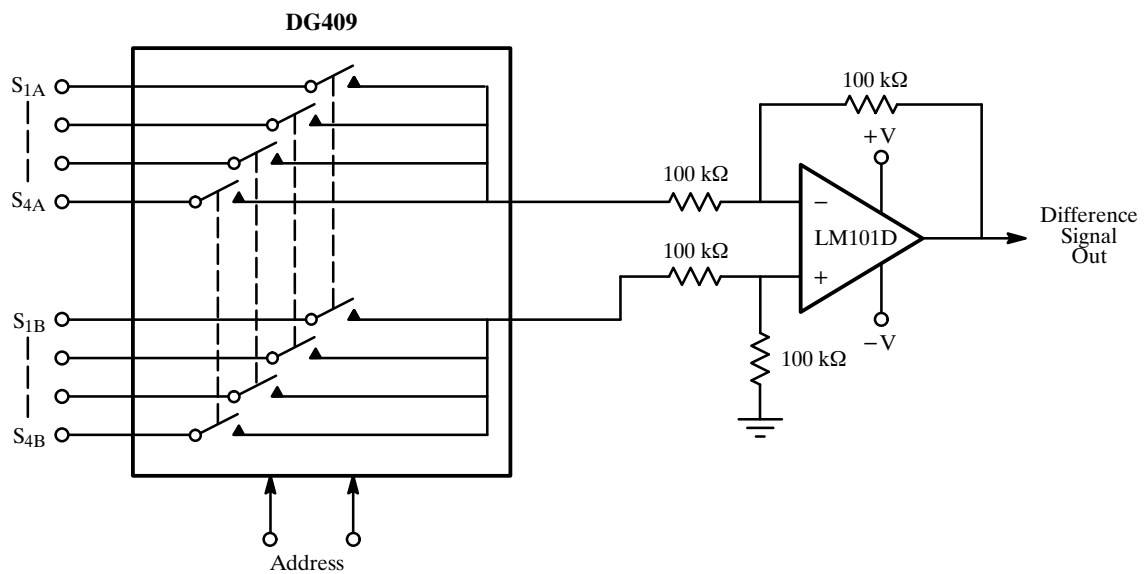
Figure 3. CMOS Switch Showing Inherent Diodes

Figure 4. Differential Multiplexer

High-frequency signals above a couple of MHz can limit system accuracy, whether its specific channel is on or off. When the device is turned on, the signal is filtered to some degree by the distributed resistance and capacitance of the signal path through the multiplexer. When the device is turned off, the high frequency couples with adjacent channels through the "off" channel to the output, thereby adding to the system error.

What Makes the DG408/409 a Good Multiplexer?

Choosing a technology for a multiplexer can depend on many factors, including the environment, its ruggedness, the accuracy required, and the cost. The choice is often a compromise between these factors. The DG408/409 is fabricated with high-voltage CMOS technology developed specifically by Siliconix to enhance the analog switch/multiplexer range. The processing steps include a buried layer which prevents the formation of the inherent SCR found in CMOS structures. This immunity to latch-up makes the DG408/409 particularly insensitive to transient conditions which could occur in a remote multiplexer environment.

Figure 5 shows a typical profile, including the inherent parasitic components. Under specific conditions (inputs exceeding the supplies), one or more of the pn junctions becomes forward biased and, under normal conditions, would result in the pnpn structure turning on. This would appear as a short circuit across the supply and would persist until the power was removed or the device burned up.

Using the "buried layer", the gain of the pnpn structure has been reduced to less than unity. This effect makes device latch-up virtually impossible.

Accuracy

Errors introduced by a multiplexer can be split into dc and ac components. Steady-state errors in a multiplexer are due to the on-resistance and finite leakage of the switch. Two sources of dc error can be quantified by

$$\text{input offset} = R_S \times I_{S(\text{off})}$$

where

R_S = source resistance
I_S = source leakage
$r_{DS(\text{on})}$ = on-resistance
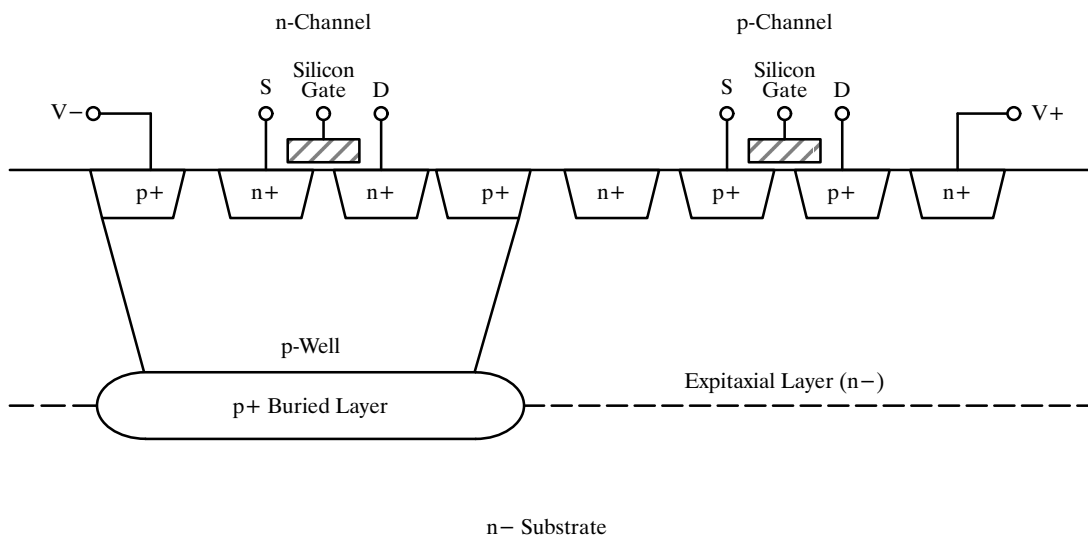$I_{D(\text{on})}$ = drain on-state leakage.

Figure 5.   Cross Section of a High Voltage Silicon Gate CMOS Device

Multiplexer

$r_{DS(on)}$

$I_{D(on)}$

Thermo Couple

Strain Gauge

I_{BIAS}

Amplifier

Reference Voltage

DG408

A/D Converter

Link

Processor

Demultiplexer

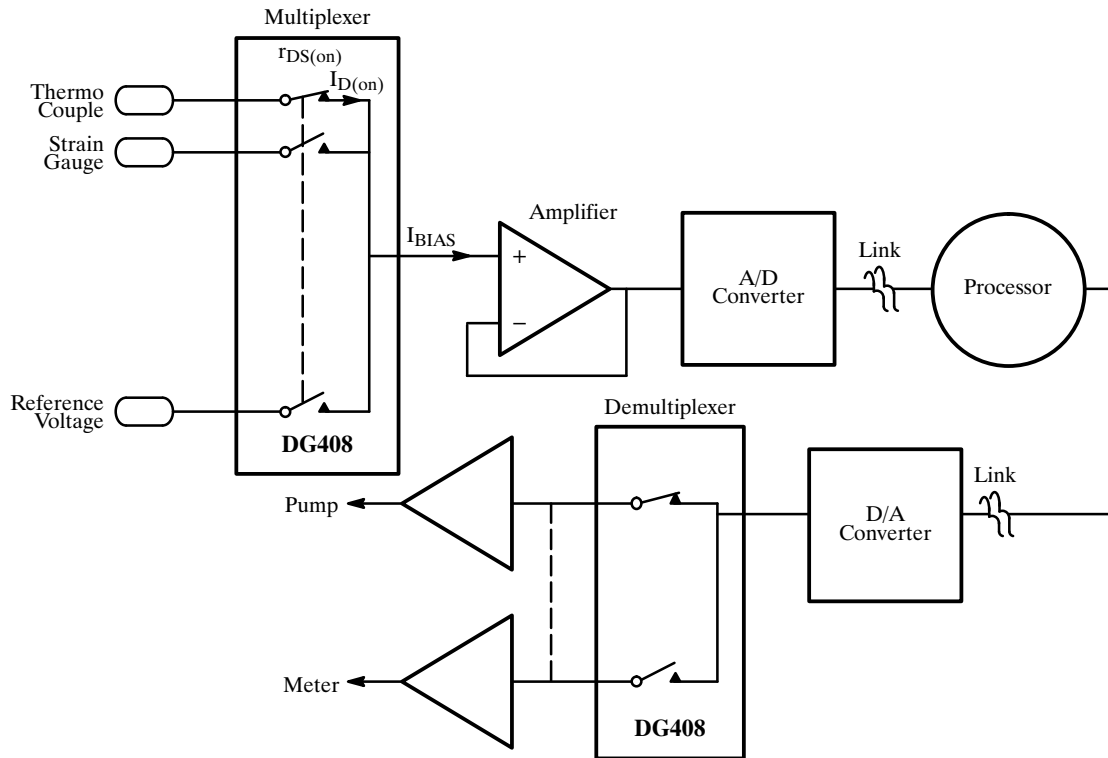Pump

Link

D/A Converter

Meter

DG408

Figure 6. Typical Data Aquisition System

Figure 6 shows a typical data multiplexing system. Because the multiplexer feeds a very high impedance, its input offset is a function of its on-resistance and the on-state leakage of the switch plus the amplifier bias current.

$$V_{OFFSET} = r_{DS(on)} \times (I_{D(on)} + I_{(BIAS)})$$

For the DG408/409 typical specifications, this offset will be

$$V_{OFFSET} = 100 \times (500\,pA + 30\,pA) = 53\,nV$$

R_{SOURCE}

V_{SOURCE}

DG408

V_O

10 nF

$V_{SOURCE} = 0\,V$
$R_{SOURCE} = 0\,\Omega$

V_O

ΔV_O

Address

SW Off

Switch On

SW Off

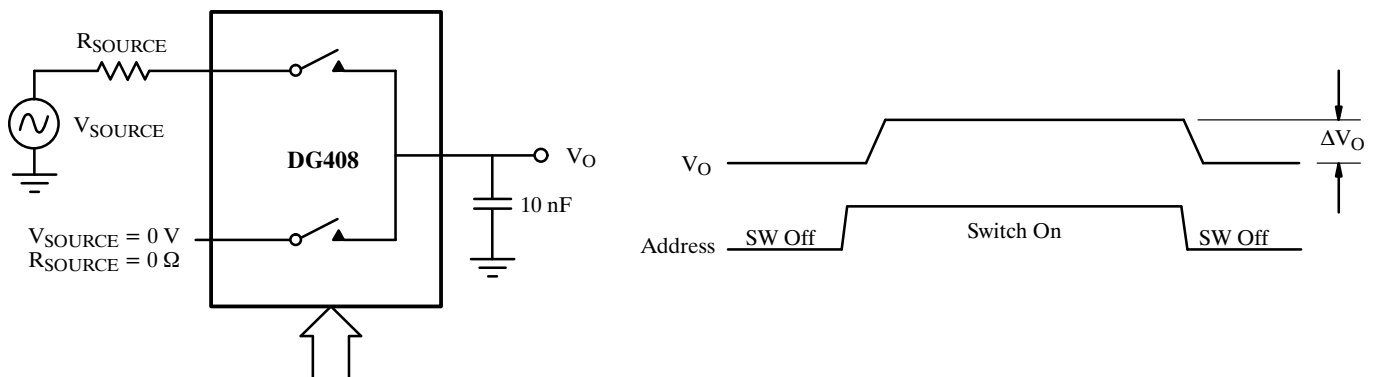**Figure 7.** Charge Injection Test Circuit

This typical offset (at 25°C) should be compared with the signal level to determine whether the error introduced by the offset is acceptable.

Another source of error that may be introduced by the switch occurs when the switch changes state. Transients (due to capacitive coupling between the drivers and drain) can be manifested as an error voltage appearing on the output node. The effect of charge injection is measured in volts and is given by

$$V = Q_i/C$$

where

Q_i is the injected charge in picocoulombs

C is the load capacitance at the output.

The DG408/409 devices have been internally compensated to minimize the effects of the injection. This is achieved by including compensation capacitors on the output switch. These capacitors are sized to produce an equal and opposite transient which tends to cancel out the effect of the switch injection. Typical charge injection for the DG408/409 is 20 pC for the test configuration shown in Figure 7.

Switching Speed

Multiplexers operate in real time (i.e., samples are taken sequentially and represent the analog input signal). Obviously, the quicker a multiplexer changes state, the more samples can be taken in a given time. Fast switching operation is often difficult to achieve using larger multiplexing devices. That is, the greater the number of channels, the slower the speed due to additional capacitance at the common output node.

The DG408/409 switching speed (t_{TRANS}) is 250 ns maximum at room temperature with a 10-ns minimum break-before-make time. While this break-before-make time prevents overlap or "alias" between channels, it reduces multiplexer efficiency and, therefore, is kept as short as possible.

A channel-switching rate (Figure 8) is defined for the DG408/409 by t_{ON}, t_{OFF}, and t_{SAMPLE}, where t_{SAMPLE} is dependent on the application.

Assuming a t_{SAMPLE} of 1.2 μs, the maximum switching rate for the DG408/409 (with no pulse-edge overlap) is once every 1.5 μs or a frequency of 666 kHz. This example shows that the switching speed of the DG408/409 is not a significant factor unless the t_{SAMPLE} time becomes much smaller. For multi-channel systems, if the sampling theorem is obeyed, the maximum switching rate will limit the number of channels and/or the maximum frequency components of any of the channel inputs. Techniques are available to improve the switching rate, and an example using the DG408/409 and DG400 will be shown later.

Versatility

With CMOS switches, signal conduction is the same in either direction. Therefore, as shown in Figure 9, it's possible to use the DG408 as a *demultiplexer* with one input from the digital-to-analog converter and 8 outputs.

This versatility allows the same advantages at the "back end" of the system—that is, a single wire can be used to carry all the control signals to the remote site. Then the control signals may be converted back to analog form and demultiplexed for controlling the system.
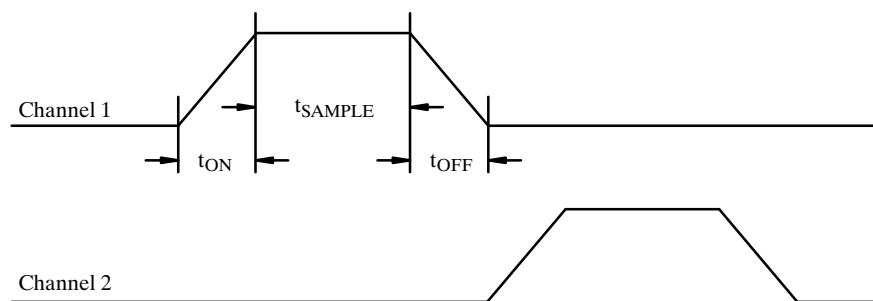

Figure 8. Channel Switching Rate

Logic Compatibility

The compatibility of the multiplexer is a measure of how easy it is to interface with other system components, such as transducers, A/D converters, power supplies, the environment, etc.

The DG408/409 has many features which make this interfacing as easy as possible. For example, a regulator has been included on the chip to provide stability against power supply and temperature variations. The regulator maintains TTL compatibility over power supply variations, while the dynamic specifications can be met over the full military temperature range. The regulation also guarantees a low current consumption of ± 75 μA, making it suitable for battery/portable applications.

Application Enhancements

The following examples of applications using the DG408/409 are intended to highlight some specific improvements over their predecessors.

Sample-and-hold circuits using analog multiplexers are widely used in analog signal processing and data conversion systems to store analog voltages accurately over time periods ranging from nanoseconds to several minutes. This ability finds many applications, including data distribution systems, simultaneous sample-and-hold designs, sampling oscilloscopes, digital volt meters, signal reconstruction filters, and analog computational circuits. Although they are
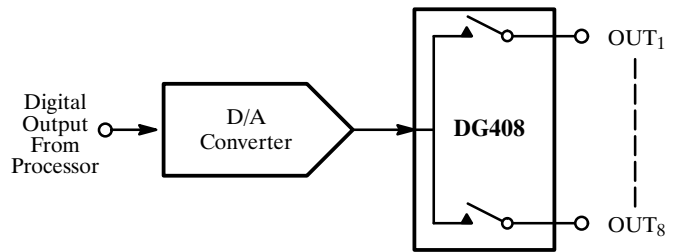
Figure 9. Using the DG408 as a Demultiplexer

theoretically simple, these high-speed, high-accuracy circuits need careful consideration in their design. Figure 10 shows the DG408 in a sample-and-hold circuit. During the sample phase, one switch in the analog multiplexer is closed and the hold capacitor is charged to the input voltage via the on-state switch. Once the capacitor is charged to its final value, the hold mode is entered by opening the switch.

During the hold mode, the capacitor voltage can be examined via the low-leakage buffer. By repeating this with other switches in the multiplexer, many analog inputs can be sequentially examined.

In a high-speed system, an important specification for the circuit designer is the acquisition time of the sample-and-hold system—that is, the time delay between the sample command and the capacitor reaching its final value.
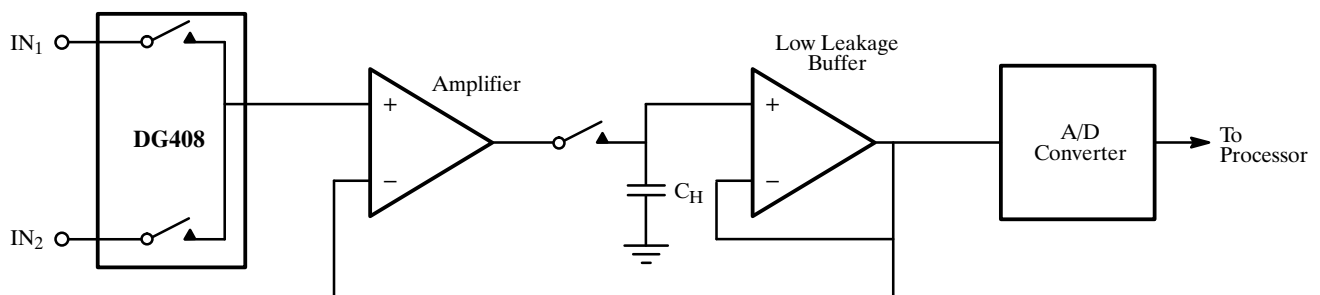
Figure 10. High Performance Sample/Hold Circuit

7

Figure 11 shows that the acquisition time is dependent on two factors. The first factor is the time from when the sample command is given to when the switch is turned on (i.e., the t_{on} of the switch). For the DG408, the t_{on} is guaranteed as 250 ns maximum at 25°C; this translates to a 4 times improvement over existing pin-compatible devices.

The second contribution to acquisition time is the time taken for the hold capacitor to charge to its final value. The charging time is determined by the source impedance of the analog source, the on-resistance of the switch, and the hold capacitor. Hence, for low-impedance analog sources, the on-resistance of the switch will play an important part in determining the time constant. The on-resistance of the DG408/409 is guaranteed at 100 Ω over the whole analog voltage range, making a 500% improvement over existing pin-compatible parts.

To illustrate the improvements in acquisition time made possible with the DG408/409, consider the following comparison with the DG508A pin-compatible multiplexer. The acquisition time is

$$t_A = t_{on} + n \times (R_S + r_{DS(on)}) \times C_H$$

where n is the number of time constants (determined by the accuracy required).

R_S is the source resistance of the analog input while C_H is the hold capacitor.

If

$C_H = 100$ pF
$R_S = 50$ Ω
$n = 10$

then for the DG508A,

$t_A = 1.5$ μs + $10 \times (50 + 450) \times 100$ pF
$t_A = 1.5$ μs + 500 ns
$t_A = 2$ μs.

Using the same conditions for the DG408,

$t_A = 250$ ns + $10 \times (50 + 100) \times 100$ pF
$t_A = 250$ ns + 150 ns
$t_A = 400$ ns.

Thus, by using the DG408, the acquisition time is improved by 5 times.

For high-accuracy systems, an important consideration is the sample-to-hold offset error. This error arises when the
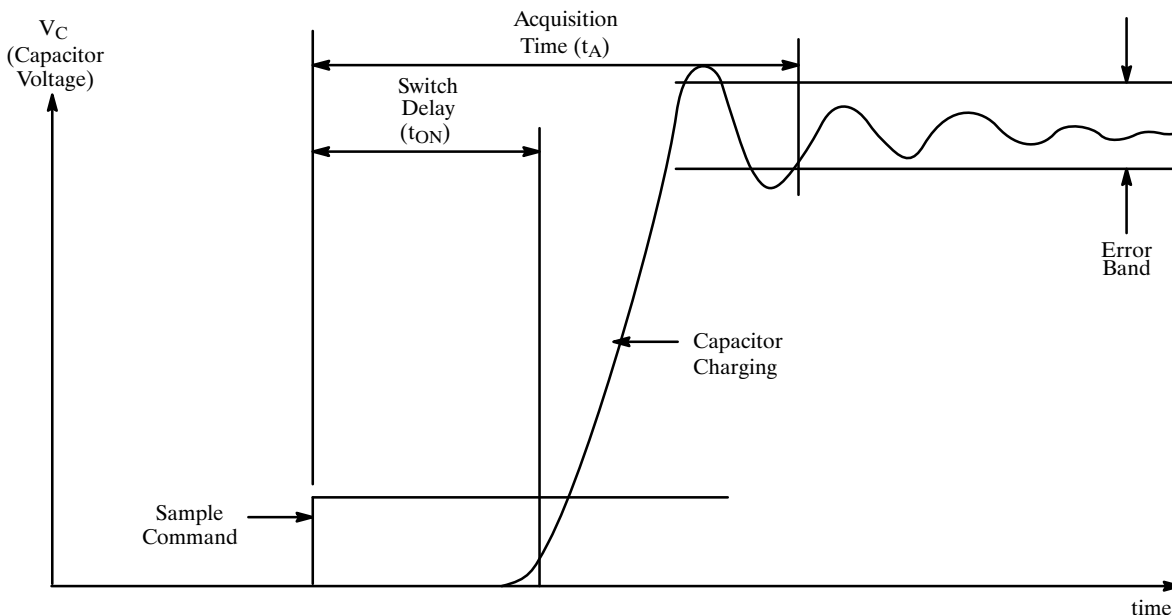

Figure 11. Acquisition Time of a Sample/Hold System

switch turns off and charge is injected by the switch onto the hold capacitor, adding an error to the stored analog voltage. The error is related to the hold capacitor by

$$V_O = Q_i/C_H$$

where

V_O is the offset error
Q_i is the injected charge
C_H is the hold capacitor.

As an example of the possible improvement with the DG408, a comparison is drawn with the DG508A. Assuming a 1-nF hold capacitor, for the DG508A,

$$V_O = 50 \, pC \div 1 \, nF = 50 \, mV$$

and for the DG408,

$$V_O = 20 \, pC \div 1 \, nF = 20 \, mV.$$

Thus, a 2.5-fold improvement in error voltage is provided by using the DG408.

The ability of the system to store the analog sample when the switch goes off is referred to as the droop rate. It is measured as the change in voltage versus time while in the hold mode. The droop rate depends on bias current of the amplifier, the leakage of the capacitor, and the off-state leakage of the multiplexer. The low-leakage performance of the DG408/409 allows a lower droop rate (i.e., a more accurate storage of the analog sample).

High-Speed Switching

In large segments of the electronics industry, speed is a primary concern in product design. Computer graphics, video equipment, and medical electronics are a few examples where high-speed switching is required. The activation frequency of a multiplexer (i.e., the frequency at which the switch can be toggled) is directly related to the switching speed of the device (i.e., the faster the switching speed, the higher the activation frequency). The DG408 has guaranteed maximum of 250 ns switching speed, thus making it theoretically possible to toggle the switch up to 2 MHz. Figure 12 shows how a two-level multiplexer can be used to increase the data transmission rates in an analog multiplexed system.
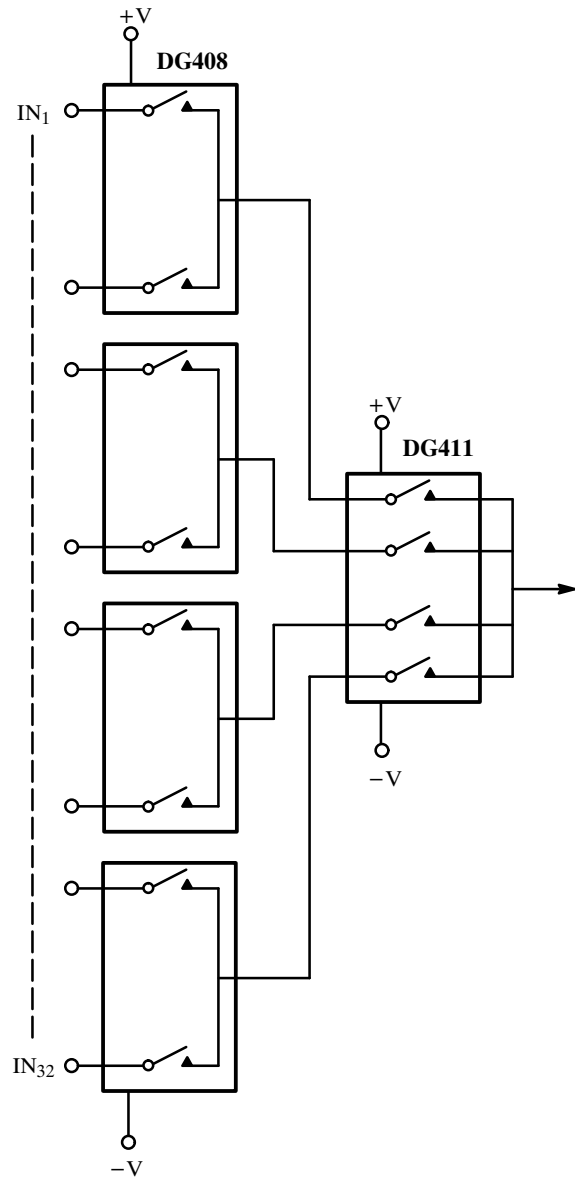

Figure 12. Two-Level Multiplexing with the DG408

Use of the two-level system gives improved performance over a single-level system. Examples of these improvements are listed below.

● Output capacitance results only from the second-level device and not from the sum of the first-level devices.

● The leakage currents at the output node will be reduced from the sum of the second-level devices to that of the second-level device.

● In a design where one multiplexer is sampled while the other is switched, the switching speed of the system is increased to that of the DG400.

- Crosstalk and isolation are improved because one-half of the system will have two off switches in series to the output node at any given time.

Differential Multiplexing of Low-Level Signals

When multiplexing low-level signals, careful choice of a multiplexer and handling of the system layout helps avoid signal masking by ac noise pick-up and dc voltages generated by thermocouple effects. To transmit the signal effectively, several factors must be considered.

- Single-ended or differential signal paths
- Low-level transmission or preamplification
- The type of conductor

The choice between a single-ended (DG408) or differential (DG409) multiplexer is really a function of the system. Cost will dictate a single-ended connection, and for a high signal level, the shorter distance should provide a stable-environment system. For a system that has a significant signal path length and is potentially being routed in a noisy environment (e.g., motors), common-mode signals can be picked up. For low-level signal transmission, this common-mode signal will provide a significant error. To minimize the effect of the common-mode signals, a twisted pair of wires feed a differential multiplexer, such as the DG409, which is buffered by a differential amplifier that rejects the unwanted common-mode portion of the signal (see Figure 13).

The advantages of low-level or high-level transmission is again dictated by system configuration and cost. Preamplification at the transducer will provide low source impedance and voltage gain, but it introduces the problem of supplying power to the amplifier.

The transmission cable carrying the transducer signal is critical in a low-level system; it should be as short as practical. Signal conductors should be tightly twisted for minimum enclosed area. This technique guards against picking up electromagnetic interference and shields the twisted pair of wires against capacitively-coupled (electrostatic) interference. A key requirement for the transmission cable is that it presents a balanced line to the source of noise interference. This requires an equal series impedance in each conductor and an equally distributed impedance from each conductor to ground. The result should be that noise will be coupled in phase to both conductors and rejected as common-mode voltages. Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also ground loops are produced if the shield is grounded at both ends by standard baby "N" connector sockets. If coaxial cable is used, the signal should be carried on the center conductors of two equal-length cables whose shield is terminated only at the transducer end.

Silicon in contact with aluminum creates a thermocouple voltage. In a typical multiplexer, the source voltage will be exactly canceled by the drain voltage, but large thermal gradients between source and drain contacts can produce a net offset voltage. The low current consumption of the DG409 (± 75 μA) translates into minimal errors due to thermocouple offsets.
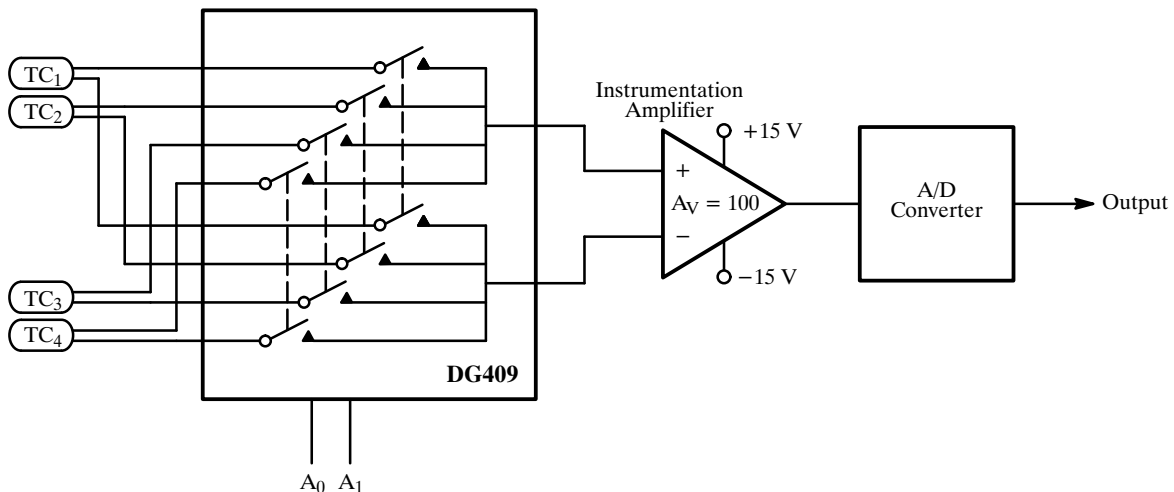

Figure 13. Differential Multiplexing of Thermocouples

Programmable Amplifier

Figure 14 shows a programmable amplifier with selectable inputs. This configuration is used in auto-ranging digital volt meters, signal conditioners, etc. Its purpose is to select optimum gain ready for conversion.

Gain ratios are a function of the resistor ratios. Sources of error will be due to the on-resistance of the switches contributing to the resistor ratio. The low on-resistance of the DG408 (typically 40 Ω at 25°C) and close matching should minimize ranging errors introduced by the switches. The switching speed of the DG408 will allow the preferred value of gain to be attained quickly.

Conclusion

For multiplexers to maintain their usefulness in high-performance systems, their design must incorporate the latest technological advances. As digital controllers are becoming faster and analog sources more accurate, the modern multiplexer must reflect these advances to become a stronger link in the transition from the analog to the digital world. The DG408 and DG409 are designed to meet these new requirements in the marketplace and reflect Siliconix' commitment to serve our customers' needs for state-of-the-art technology.

References

Analog Switches and Their Applications, Siliconix, June 1980.

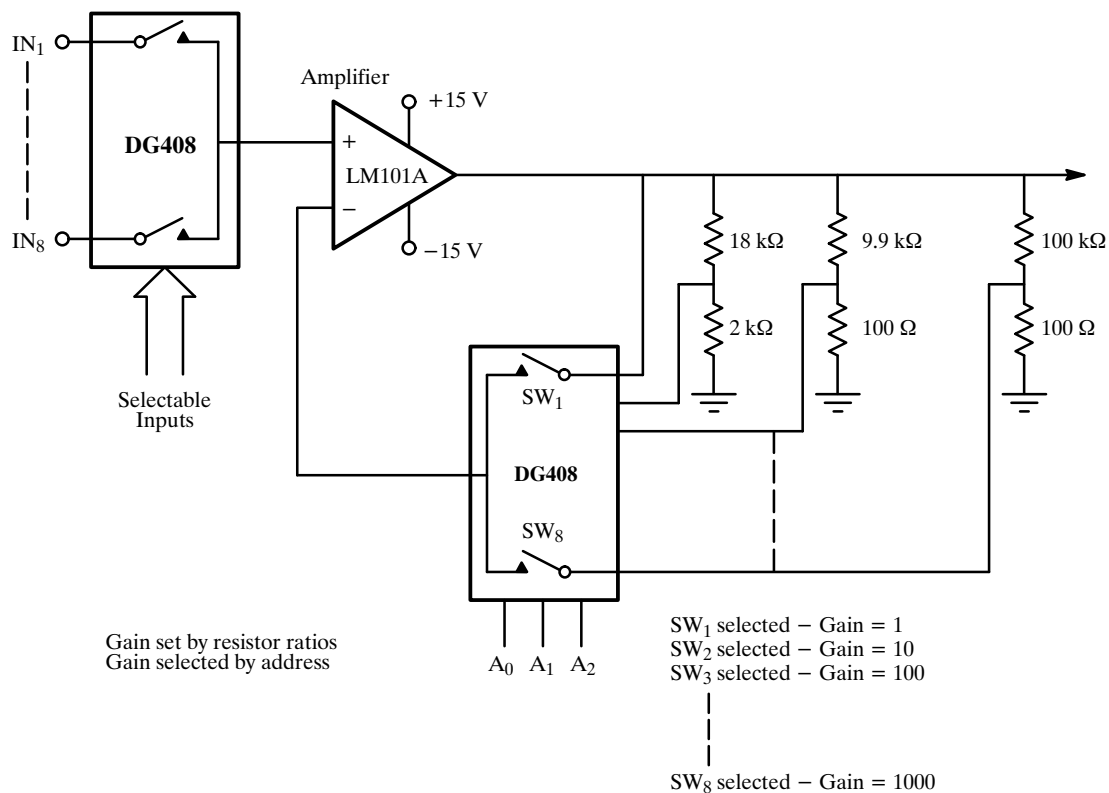Bylanski, P., *Digital Transmission Systems*, Peter Peregrinus, Ltd., 1976.

Figure 14. Programmable Amplifier with Selectable Inputs